CARRY GENERATION IN ADDRESS CALCULATION

ABSTRACT OF THE DISCLOSURE

Embodiments are provided in which the generation of a carry of a sum of two numbers can be implemented by adding only some most significant bits of the two numbers and assuming that the sum of the remaining bits do not generate a carry. Other embodiments are also provided in which the generation of the carry of a sum of the two numbers can be implemented using carry look-ahead techniques wherein generate and propagate terms are generated. By combining the product terms of the carry function and combining pairs of propagate or generate terms, the generation of the carry of the sum of the two numbers can be implemented in an And-Or-Inverter function less complex than that of prior art. Still other embodiments are provided in which one operand of a carry generation circuit comes from a fixed source and the other operand is selected from several forwarding sources. As a result, the selection of the operands and the generation of the propagate and generate terms for generating the carry can be implemented in a single complex domino level of logic which includes a sum of product followed by a simple two-way gate.